IN THE SPECIFICATION

Please amend the paragraph beginning at page 8, line 6 as follows:

Referring now to Figure 1 there is illustrated a block diagram of a constant velocity sampled retract system in accordance with exemplary embodiments of the present invention. In a "float" phase the VCM is disconnected from the driver stage so that the currents in the VCM can decay. The BEMF is sampled during the float phase using a ~~differential~~ BEMF amplifier ~~arrangement~~ 11 and provided to the PI-controller 12. A ~~further circuit~~ TBEMF generator 13 is used to ~~generated~~ generate the target BEMF (TBEMF) which is also provided to the controller 12. The controller 12 calculates the actual error, integrates it, and outputs the sum of the integrator and a proportional part. The sum is provided to an output driver 14 which provides drive currents to the VCM.

Please amend the paragraph beginning at page 8, line 18 as follows:

Referring now to Figure 2 there is shown a diagram of an SC integrator in accordance with exemplary embodiments of the present invention. The difference between BEMF and TBEMF (the actual error) is sensed on capacitor 21 in phase 1 while switches 25A and 25B are closed. At the end of this phase the switches 25A and 25B are opened and the charge on C21 is proportional to the error and the capacitor value. Subsequently, the capacitor 21 is switched between the negative and positive input of the operational amplifier 23 in phase 2 ~~2using~~ using switches 26A and 26B. During this phase, because the opamp attempts to regulate its input differential voltage to 0, effectively all the charge is transferred from C21 to C22. At the end of phase 2 the switches 26A and 26B are opened and the cycle starts over with phase 1. Doing this continuously integrates the error at the input on capacitor 22.

Please amend the paragraph beginning at page 9, line 11 as follows:

Referring now to Figure 3 there is shown an SC controller based on the SC integrator shown in Figure 2 in accordance with exemplary embodiments of the present invention. Two components have been added to the integrator of Figure 2: a capacitor 31 connected from the positive input of the amplifier to VREF and a parallel reset switch 32. Sampling works basically as before. The input (error) voltage is stored on the sampling capacitor 21 and in addition the reset switch 32 is closed in order to discharge the capacitor 21 and connect the ~~opamp~~ operational amplifier 23 to VREF. In the storage phase, the sampling capacitor 21 is connected to the opamp inputs again and the reset switch 32 is opened. Still the opamp 23 tries to regulate the input voltage to zero and integrates the charge on the feedback capacitor 22. But this time the charge also is stored on the third capacitor 31 which provides a common mode signal to the system. This common mode signal is proportional to the input voltage and the ratio of the sampling capacitor 21 to the third capacitor 22 (this is effectively the proportional part K_P as shown in Figure 1). The output signal finally is that proportional part plus the voltage across the integrating capacitor 22 (this is effectively the integral part K_I as shown in Figure 1).

Please amend the paragraph beginning at page 10, line 7 as follows:

Referring now to Figure 4 there is shown an SC controller with error cancellation in accordance with exemplary embodiments of the present invention. System error can come from, for example, the input offset of the BEMF amplifier 11 (Figure 1) and the TBEMF generation 13 (Figure 1) and integrator and operational amplifier 23 (Figure 2). For the error cancellation two additional phases are introduced to the circuit illustrated in Figure 3 and effectuated by the switches shown as items 41-44. They basically can be seen as another sample and storage phase which senses the system error and stores it with the opposite sign, so that it can be used to cancel the error made in the "real" sampling phase.

Please amend the paragraph beginning at page 10, line 19 as follows:

In the calibration phase the switches 42a,43,41A,41D are closed all the time. Switch 44 is open all the time to avoid destroying the charge on capacitor 22. By closing switch 32 the offset of the BEMF amplifier at 46 (where the amplifier inputs are shorted to VREF during this time) is switched to the positive input of the integrator opamp 23. Opamp 23 is switched into buffer using switch 43 and switches 41A, 41D, 25A and 25B are configured to store the difference between the output voltage of ~~opamp~~ operational amplifier 23 and Vref on capacitor 21. At the end of this phase the switches 25A, 25B and 32 are opened. In the drive phase the switches 26A and 26B are closed and the charge on capacitor 21 is transferred to capacitor 31. This one now has stored both the offset of the BEMF amplifier and the offset of ~~opamp~~ operational amplifier 23. At the end of this phase 26A and 26B are opened again.